UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/841,077	04/25/2001	Masashi Yamawaki	02416-00008	5889

			EXAMINER

7590   12/13/2006

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EXAMINER
TORRES, JUAN A

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 12/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/841,077	YAMAWAKI, MASASHI
	Examiner	Art Unit	
	Juan A. Torres	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2006*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7, 9-16, 18 and 19* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 9-16, 18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/02/2006 has been entered.

Claim Objections

The modifications to the claims were received on 10/02/2006. These modifications are accepted by the Examiner.

In view of the amendment filed on 10/02/2006, the Examiner withdraws the claim objections of claim 12 of the previous Office action.

Claims 1-7, 9-10 and 18-19 are objected to because of the following informalities:

As per claim 1, the recitation in line 3 of claim 1 "; and" is improper, because there are still two more limitations in the claim (see claim 11 lines 4 and 5); it is suggested to be changed to ";".

As per claim 10, the recitation in line 6 of claim 10 "; and" is improper, because there are still two more limitations in the claim (see claim 11 lines 4 and 5); it is suggested to be changed to ";".

As per claims 2-7, 9 and 18, they are objected because they depend directly from claim 1 and claim 1 is objected.

As per claim 19, it is objected because it depends directly from claim 10 and claim 10 is objected.

Appropriate correction is required.

Response to Arguments

<u>Regarding claims 1 and 10:</u>

The Applicant contends, "the apparatus and method of Wilson cannot and do not detect a predetermined mark for synchronization by any <u>one</u> detecting unit, as recited in claims 1 and 10, nor is a predetermined mark detected from any <u>one</u> of strings of bits of the parallel data continuing from each bit position of the parallel data to establish synchronization of the series of data, as recited in claim 11".

The Examiner disagrees, and asserts, that as indicated in the previous Office action Wilson discloses a plurality of detecting units 524 to 518 included in blocks 515 and 516 to detect Marks_0 and Mark_1 respectively, and any one of this detecting units can detect a predetermined mark for synchronization, Mark_0 and Mark_1 respectively.

For these reasons and the reason stated en the previous Office Action, the rejection of claims 1 and 10 are maintained.

<u>Regarding claim 11:</u>

The Applicant contends, "the apparatus and method of Wilson cannot and do not detect a predetermined mark for synchronization by any <u>one</u> detecting unit, as recited in claims 1 and 10, nor is a predetermined mark detected from any <u>one</u> of strings of bits of the parallel data continuing from each bit position of the parallel data to establish synchronization of the series of data, as recited in claim 11".

The Examiner disagrees, and asserts, that as indicated in the previous Office action Wilson discloses a plurality of detecting units 524 to 518 included in blocks 515 and 516 to detect Marks_0 and Mark_1 respectively, and any one of this detecting units can detect a predetermined mark from any one of the string of bits of the parallel data counting from each bit position of the parallel data to establish synchronization of the series of data.

For these reasons and the reason stated en the previous Office Action, the rejection of claim 11 is maintained.

Regarding claims 2-7, 9, 12-16, 18 and 19:

The Applicant contends, "For at least these reasons, the Applicants submit that independent claims 1, 10 and 11, as amended, are allowable over Wilson. As claims 1, 10 and 11 are allowable, the Applicants submit that claims 2-7, 9, 12-16, 18 and 19, each of which depends from one of allowable claims 1, 10 and 11, are likewise allowable for at least the reasons set forth above with respect to claims 1, 10 and 11".

The Examiner disagrees, and asserts, that because the rejection of claims 1, 10 and 11 are maintained, the rejection of claims 2-7, 9, 12-16, 18 and 19 are also maintained.

For these reasons and the reason stated en the previous Office Action, the rejection of claims 2-7, 9, 12-16, 18 and 19 are maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 9-16, and 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Wilson (US 6118603 A).

As per claim 1, Wilson discloses a receiving unit for receiving a series of data including a predetermined mark for detecting synchronization and generating parallel data from the series of data (figure 5 input block 510 line 508 column lines 7 lines 48-52); and a plurality of detecting units being provided at each bit position of the parallel data, the detecting units being adapted to detect whether strings of bits of the parallel data corresponding to strings of bits of the series of data from each bit position of the parallel data as a starting point of the predetermined mark are the predetermined mark (figure 5 blocks 515 and 516 column 8 lines 12-23, Wilson discloses a plurality of detecting units 524 to 518 provided at each bit position, included in blocks 515 and 516 to detect Marks_0 and Mark_1 respectively, and any can detect a predetermined mark for synchronization, Mark_0 and Mark_1 respectively); and where any one of the detecting units detects the starting point of the predetermined mark (figure 5 blocks 515 and 516 column 8 lines 12-23 and 34-46).

As per claim 10, Wilson discloses a data processor for detecting a predetermined mark for detecting synchronization that is included in a series of data read from a memory medium in order to establish synchronization at a time of transferring the series

of data to a controller unit from a read channel unit, comprising a receiving unit for

receiving the series of data including the predetermined mark for detecting

synchronization and generating parallel data from the series of data (figure 5 input block

510 line 508 column lines 7 lines 48-52); and a plurality of detecting units being

provided at each bit position of the parallel data, the detecting units being adapted to

detect whether strings of bits of the parallel data corresponding, to strings of bits of the

series of data from each bit position of the parallel data as a starting point of the

predetermined mark are the predetermined mark (figure 5 blocks 515 and 516 column 8

lines 12-23, Wilson discloses a plurality of detecting units 524 to 518 provided at each

bit position, included in blocks 515 and 516 to detect Marks_0 and Mark_1 respectively,

and any can detect a predetermined mark for synchronization, Mark_0 and Mark_1

respectively); and wherein any one of the detecting units detects the starting point of the

predetermined mark (figure 5 blocks 515 and 516 column 8 lines 12-23 and 34-46).

As per claim 11, Wilson discloses a data processing method comprising the

steps of receiving a series of data including a predetermined mark for detecting

synchronization (figure 5 input block 510 line 508 column lines 7 lines 48-52);

generating a parallel data from the series of data (figure 5 output of block 520 input of

blocks 515 and 516 column 7 lines 53-58); detecting the predetermined mark for

detecting synchronization from any one of strings of bits of the parallel data continuing

from each bit position of the parallel data to establish synchronization of the series of

data (figure 5 blocks 515 and 516 column 8 lines 12-23, Wilson discloses a plurality of

detecting units 524 to 518 provided at each bit position, included in blocks 515 and 516

to detect Marks_0 and Mark_1 respectively, and any can detect a predetermined mark

for synchronization, Mark_0 and Mark_1 respectively); and demodulating the series of

data based on the predetermined mark for detecting synchronization detected from one

of the bit strings (figure 5 blocks 538 and 556; column 8 lines 12-65 and column 11 lines

8-16).

As per claims 2 and 12, Wilson discloses claims 1 and 11. Wilson also discloses

detecting the predetermined mark for detecting synchronization in a predetermined bit

width among the series of data in parallel condition (figure 5 blocks 515 and 516 column

7 lines 53-56; and column 8 lines 13-65).

As per claims 3 and 13, Wilson discloses claims 1 and 11. Wilson also discloses

generation timing for selecting generation timing of the window for detecting the

predetermined mark based on the predetermined mark for detecting synchronization

(figure 5 block 506 column 7 lines 44-46).

As per claim 4, Wilson discloses claim 1. Wilson also discloses a data

demodulating unit for demodulating the series of data between the predetermined mark

for detecting synchronization based on the predetermined mark for detecting

synchronization (figure 5 block 556 column 11 lines 8-16).

As per claims 5 and 14, Wilson discloses claims 1 and 11. Wilson also discloses

a detection line memory for storing a detection line based on the predetermined mark

for detecting synchronization (column 11 line 66 to column 12 line 8).

As per claims 6 and 15, Wilson discloses claims 1 and 11. Wilson also discloses selecting data based on the predetermined mark for detecting synchronization (figure 5 block 564 column 11 lines 54-65).

As per claims 7 and 16, Wilson discloses claims 1 and 11. Wilson also discloses counting the series of data between the predetermined mark for detecting synchronization based on the predetermined mark for detecting synchronization (figure 5 block 542 and figures 6 and 7 column 9 lines 15-23).

As per claim 9, Wilson discloses claim 1. Wilson also discloses a shift register to input the plurality of parallel bits connected with the detecting units in the same number as the number of parallel data (figure 5 block 510 column 7 lines 56-58; and column 8 lines 13-65).

As per claims 18 and 19, Wilson discloses claims 1 and 10. Wilson also discloses that the plurality of detecting units are provided in equal number to the number of bits constituting the parallel data (figure 5 block 518; column 8 lines 47-54).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Juan Alberto Torres
11-15-2006